REMARKS

Applicant thanks the Examiner for the thorough examination of the application. No new matter is believed to be added to the application by this Amendment.

Status of the Claims

Claims 1-16 are pending in the application. The amendments to the claims improve their language.

Objection to the Drawings

The Examiner objects to Figure 7 as not properly designating "CLK3." Amended Figure 7 properly designates "CLK3."

Claim Objections

The Examiner objects to claims 9, 10, 13 and 15 as containing informalities. The claims, as amended, are free from informalities.

Rejection Under 35 U.S.C. §103(a) Over Uchino and Nakano (and Itakura)

Claims 1, 3-5, 7-9 and 11-16 are rejected under 35 U.S.C. §103(a) as being obvious over Uchino (U.S. Patent 6,040,816) in view of Nakano (U.S. Patent 6,529,181). The Examiner adds the

teachings of Itakura (U.S. Patent 5,252,957) to reject claims 2, 6 and 10. Applicant traverses.

The Present Invention and its Advantages

The present invention pertains to a novel LCD device that increases display quality by minimizing EMI (electromagnetic interference). The inventive LCD device utilizes a synchronized data sampling technology that minimizes the use of unnecessary voltage, thereby decreasing power consumption.

The present invention is typically embodied by claim 1, which sets forth:

> 1. An LCD device, comprising:
> a LCD panel;
> a plurality of source drivers applying data signals to the LCD panel;
> a plurality of gate drivers applying gate driving signals to the LCD panel;
> a timing controller outputting at least two clock signals having different phases, the timing controller separately outputting data synchronized with each output signal; and
> at least two data buses transmitting the data separately output from the timing controller to the source drivers.

As shown in Figure 4, source drivers 43 apply data signals to the LCD panel 41, and the gate drivers 45 apply gate-driving signals to the LCD panel 41. The timing controller 47 receives a data clock signal DCLK and R/G/B digital data, and outputs first and second clock signals CLK1 and CLK2 having different phases and

various control signals to control the source and gate drivers 43 and 45. The timing controller 47 connects to each source driver by a first data bus DB1 transmitting the digital data synchronized with the first clock signal CLK1 to each source driver 43, and a second data bus DB2 transmitting the digital data synchronized with the second clock signal CLK2 to each source driver 43.

Distinctions of the Invention over Uchino, Nakano and Itakura

Uchino pertains to an active matrix display device having phase-adjusted sampling pulses. Figure 1 of Uchino (relied upon by the Examiner) shows a horizontal scan circuit 20 having a shift register 20a. The scan circuit 20 scans video signals S1, S2, S3 . . . and outputs sampling pulse A1, A2, A3 . . . to logical circuits 70a, 70b, 70c . . . to disperse the sampling pulses B1, B2, B3. . .

The invention, in contrast, shows a fundamentally different driving logic. As shown in Figure 4 of the invention, the timing controller 47 feeds both clock signals CLK1, CLK2 and RGB data to source drivers 23. The timing controller 23, provides the logic that the logical circuits 70a, 70b, 70c . . . of Uchino provides, but at a fundamentally different location in the circuit.

The Examiner admits to this fundamental difference of Uchino by stating: "Uchino fails to specifically teach that the clock signals

are input to the source drivers from a timing controller. . ." Office Action at page 3, lines 17-18. The Examiner admits to further failures of Uchino, stating: "Uchino also fails to specifically teach the usage of two data buses transmitting data from the external device to the drivers . . . Uchino also fails to teach that the data synchronized with the respective clock signal for each odd/even numbered data or R/G/B date through different data busses." Office Action at page 3, lines 19-23.

The Examiner then turns to Fig. 1 of Nakano and tries to graft a fundamentally different circuit logic onto that of Uchino. This fundamentally different circuit is discussed at column 6, lines 22-43 of Nakano, which discusses a control circuit 110 controlling drain drivers 130 and gate drivers 140 "all of which are transmitted thereto from the computer side." This a marked contrast to the location of the logical circuits 70a, 70b, 70c. . . of Uchino.

As a result, a person having ordinary skill in the art could not combine Uchino and Nakano to produce the invention as embodied in independent claims 1 and 11. A *prima facie* case of obviousness has thus not been made over Uchino and Nakano. Claims dependent upon claims 1 and 11 are patentable for at least the above reasons.

Further, the invention shows unexpected results over Uchino. As discussed in paragraphs 0066 and 0067 of the specification, the invention produces a novel LCD device that increases display quality by minimizing EMI (electromagnetic interference). The inventive LCD device utilizes a synchronized data sampling technology that minimizes the use of unnecessary voltage, thereby decreasing power consumption.

In contrast, Uchino admits the disadvantages of the technology of Figure 1 (which was used by the Examiner). Uchino at column 2, lines 39-42 states: "Therefore, the sampling is performed wit a time lag from the original time at which the sampling must be originally performed, resulting in reduction of resolution and occurrence of ghost images." A person having ordinary skill would thus not turn to any of the teachings of Fig. 1 of Uchino to improve display resolution. The advantages of the invention over the applied art are thus clear.

Further, the Examiner turns to Itakura to reject dependent claims 2, 6 and 10. Itakura, however, fails to address the deficiencies of Uchino and Nakano.

As has been shown, the applied art is insufficient to allege *prima facie* obviousness over the claimed invention. Even if

obviousness could be alleged, this obviousness would be rebutted by unexpected results.

These rejections are accordingly overcome and withdrawal thereof is respectfully requested.

Prior Art Cited But Not Utilized By The Examiner

The prior art cited but not utilized by the Examiner shows the status of the conventional art that the invention supercedes. No additional remarks are accordingly necessary.

Priority

The Examiner has acknowledged priority in the Office Action Summary of the Office Action mailed October 6, 2003.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E. Goozner (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Joseph A. Kolasch, #22,463

JAK/REG/jmb:jls
0465-0883P

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

Attachment(s): Red-ink corrected copy of Figure 7
Formally corrected Figure 7

(Rev. 09/30/03)

FIG. 7